FAIRCHILD

SEMICONDUCTOR ™

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74ALVC16722
Low Voltage 22-Bit Register
with 3.6V Tolerant Inputs and Outputs

General Description

The ALVC16722 low voltage 22-bit register contains twenty-two non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The design has been optimized for use with JEDEC compliant 200 pin DIMM modules.

The 74ALVC16722 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O capability up to 3.6V.

The 74ALVC16722 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V to 3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD} (CLK to O_n)
   4.1ns max for 3.0V to 3.6V V_{CC}
   5.1ns max for 2.3V to 2.7V V_{CC}
   9.2ns max for 1.65V to 1.95V V_{CC}
- Power-off high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Meets JEDEC registered module specifications
- Latchup conforms to JEDEC JED78
- ESD performance:
   Human body model > 2000V
   Machine model >200V

Note 1: To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sourcing capability of the driver.
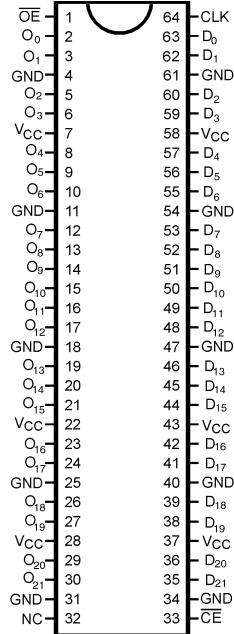
Ordering Code:

Order Number	Package Number	Package Description
74ALVC16722MTD	MTD64	64-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

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Connection Diagram

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        ┌────┐
 OE ─┤ 1    64 ├─ CLK
 O0 ─┤ 2    63 ├─ D0
 O1 ─┤ 3    62 ├─ D1
GND ─┤ 4    61 ├─ GND
 O2 ─┤ 5    60 ├─ D2
 O3 ─┤ 6    59 ├─ D3
VCC ─┤ 7    58 ├─ VCC
 O4 ─┤ 8    57 ├─ D4
 O5 ─┤ 9    56 ├─ D5
 O6 ─┤ 10   55 ├─ D6
GND ─┤ 11   54 ├─ GND
 O7 ─┤ 12   53 ├─ D7
 O8 ─┤ 13   52 ├─ D8
 O9 ─┤ 14   51 ├─ D9
O10 ─┤ 15   50 ├─ D10
O11 ─┤ 16   49 ├─ D11
O12 ─┤ 17   48 ├─ D12
GND ─┤ 18   47 ├─ GND
O13 ─┤ 19   46 ├─ D13
O14 ─┤ 20   45 ├─ D14
O15 ─┤ 21   44 ├─ D15
VCC ─┤ 22   43 ├─ VCC
O16 ─┤ 23   42 ├─ D16
O17 ─┤ 24   41 ├─ D17
GND ─┤ 25   40 ├─ GND
O18 ─┤ 26   39 ├─ D18
O19 ─┤ 27   38 ├─ D19
VCC ─┤ 28   37 ├─ VCC
O20 ─┤ 29   36 ├─ D20
O21 ─┤ 30   35 ├─ D21
GND ─┤ 31   34 ├─ GND
 NC ─┤ 32   33 ├─ CE
        └────┘
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Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{CE}$	Clock Enable Input (Active Low)
CLK	Clock Input
D_0- D_{21}	Data Inputs
O_0 - O_{21}	3-STATE Outputs

Truth Table

CLK	$\overline{CE}$	$\overline{OE}$	D_n	O_n
X	X	H	X	Z
X	H	L	X	O_n
↑	L	L	L	L
↑	L	L	H	H
L or H	L	L	X	O_n

H = Logic HIGH
L = Logic LOW
X = Don't Care, but not floating
Z = High Impedance
O_n = Previous O_n before LOW-to-HIGH Clock Transition
↑ = LOW-to-HIGH Clock Transition

Functional Description

The ALVC16722 contains twenty-two D-type flip-flops with 3-STATE standard outputs. The twenty-two flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-HIGH Clock (CLK) transition, when the Clock-Enable ($\overline{CE}$) is LOW. The 3-STATE standard outputs are controlled by the Output-Enable ($\overline{OE}$). When $\overline{OE}$ is HIGH, the standard outputs are in high impedance mode but this does not interfere with entering new data into the flip-flops.

Logic Diagram
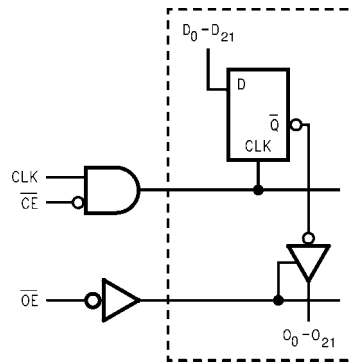
Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to 4.6V
Output Voltage (V_O) (Note 3)	−0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or GND Current per	
Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 4)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 -1.95	0.65 x V_{CC}		
			2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
V_{IL}	LOW Level Input Voltage		1.65 -1.95		0.35 x V_{CC}	
			2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	1.65 - 3.6	V_{CC} - 0.2		
		I_{OH} = −4 mA	1.65	1.2		
		I_{OH} = −6 mA	2.3	2		
		I_{OH} = −12 mA	2.3	1.7		V
			2.7	2.2		
			3.0	2.4		
		I_{OH} = −24 mA	3.0	2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	1.65 - 3.6		0.2	
		I_{OL} = 4 mA	1.65		0.45	
		I_{OL} = 6 mA	2.3		0.4	
		I_{OL} = 12mA	2.3		0.7	V
			2.7		0.4	
		I_{OL} = 24 mA	3		0.55	
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	3.6		±5.0	µA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$	3.6		±10	µA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND, I_O = 0	3.6		40	µA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	3 -3.6		750	µA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$								Units
		C_L = 50 pF				C_L = 30 pF				
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	250		200		200		100		ns
t_{PHL}, t_{PLH}	Propagation Delay CLK to Bus	1.3	4.1	2.0	5.1	1.5	4.6	2.0	9.2	ns
t_{PZL}, t_{PZH}	Output Enable Time	1.1	4.0	1.3	5.0	0.8	4.5	1.5	9.0	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	1.1	3.7	1.3	4.7	0.8	4.2	1.5	7.6	ns
t_W	Pulse Width	1.5		1.5		1.5		4.0		ns
t_S	Setup Time	2.0		2.0		2.0		3.0		ns
t_H	Hold Time	0.0		0.0		0.0		0.5		ns

Capacitance

Symbol	Parameter	Conditions		$T_A = +25°C$		Units
				V_{CC}	Typical	
C_{IN}	Input Capacitance	V_I = 0V or V_{CC}		3.3	3.5	pF
C_{OUT}	Output Capacitance	V_I = 0V or V_{CC}		3.3	5.5	pF
C_{PD}	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, C_L = 50 pF	3.3	13	pF
				2.5	13	

I_{OUT} - V_{OUT} Characteristics

I_{OH} versus V_{OH}
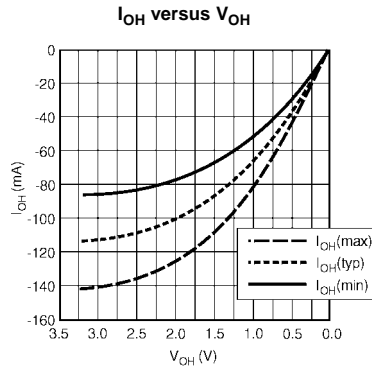
FIGURE 1. Characteristics for Output - Pull Up Driver

I_{OL} versus V_{OL}
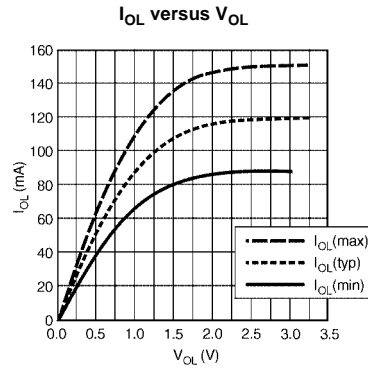
FIGURE 2. Characteristics for Output - Pull Down Driver

AC Loading and Waveforms

74ALVC16722
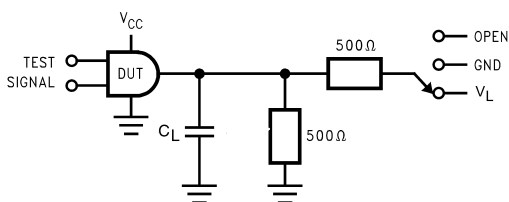
FIGURE 3. AC Test Circuit

TABLE 1. Values for Figure 1

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_L
t_{PZH}, t_{PHZ}	GND

TABLE 2. Variable Matrix
(Input Characteristics: f = 1MHz; t_r = t_f = 2ns; Z_0 = 50Ω)

Symbol	V_{CC}			
	3.3V $\pm$ 0.3V	2.7V	2.5V $\pm$ 0.2V	1.8V $\pm$ 0.15V
V_{mi}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$
V_L	6V	6V	$V_{CC}*2$	$V_{CC}*2$
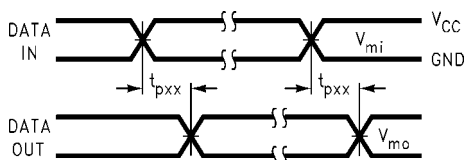
FIGURE 4. Waveform for Inverting and Non-inverting Functions
t_r = t_f $\leq$ 2.0ns, 10% to 90%
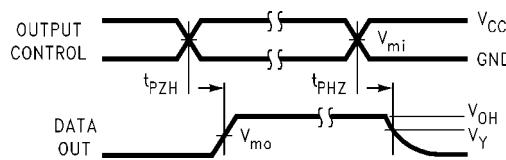
FIGURE 5. 3-STATE Output High Enable and Disable Times for Low Voltage Logic
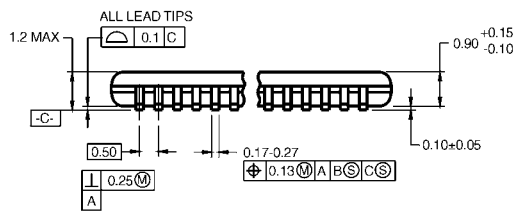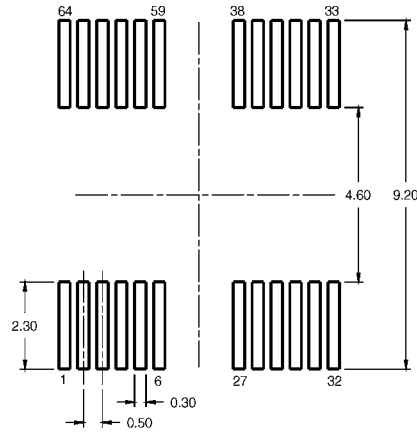t_r = t_f $\leq$ 2.0ns, 10% to 90%
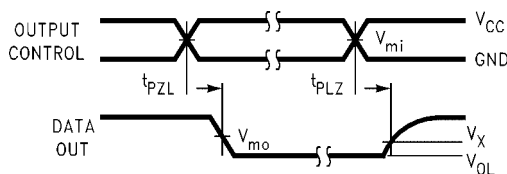
FIGURE 6. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic
t_r = t_f $\leq$ 2.0ns, 10% to 90%

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Physical Dimensions inches (millimeters) unless otherwise noted

17.00±0.10
-A-

0.65 TYP

64   33

8.10

4.05

6.10±0.10
-B-

PIN #1 IDENT.

1   32

⌒ 0.2 C B A
ALL LEAD TIPS

64   59   38   33

4.60   9.20

2.30

1   6   27   32

0.30
0.50

LAND PATTERN RECOMMENDATION

ALL LEAD TIPS

1.2 MAX   ⌒ 0.1 C

-C-

0.50   0.17-0.27

⊥ 0.25 Ⓜ
A

0.90 +0.15 -0.10

0.10±0.05

⊕ 0.13 Ⓜ A BⓈ CⓈ

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.09-0.20

12.00° TOP & BOTTOM

R0.16

GAGE PLANE

R0.31

0.25

0°-8°

0.60±0.10

1.00

SEATING PLANE

DETAIL A
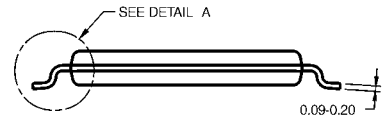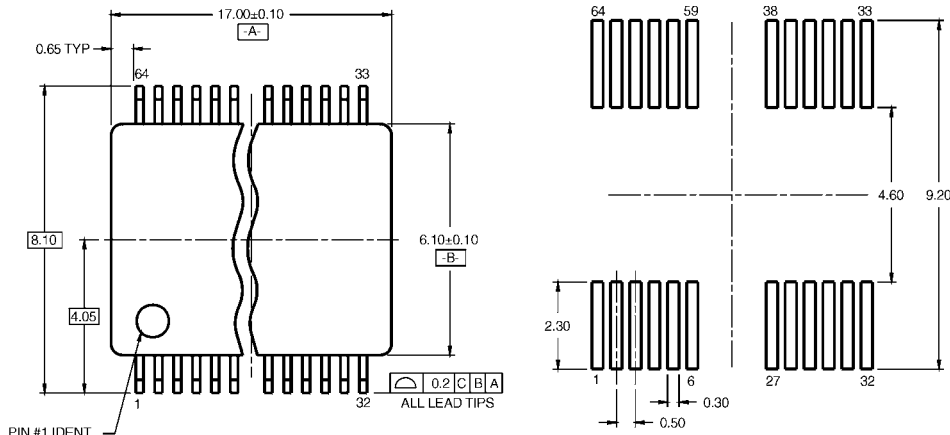
NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153,
   VARIATION EF, REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH,
   AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
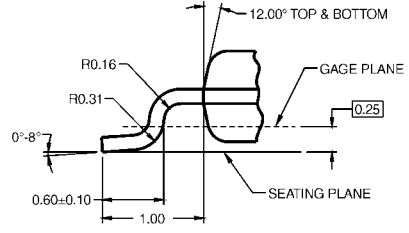
MTD64REVB

64-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD64

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